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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,798	02/25/2004	Kuo-Chi Tu	TS03-294	3345

47390 7590 04/27/2005

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,798	TU ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *13-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Applicant's election with traverse of Group I (claims1-12) drawn to a semiconductor device is acknowledged. Accordingly, claims 13-27 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method and device claims are NOT coextensive and the determinations of patentability of method and device claims are different, that is process limitations and device limitations are given weight differently in determining the patentablitity of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9, and 11-12 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,465,841 to Hsieh et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding to claim 1, Hsieh discloses a split gate flash memory cell structure for prevention of reverse tunneling comprising a semiconductor region 100 within a substrate extending to a surface; a gate insulator layer 120 formed over the semiconductor surface 100; a conductive floating gate 130 disposed over the gate insulator layer 120; a floating gate insulator layer 135 disposed over the floating gate 130 and sidewall insulator spacers 195 disposed along bottom portion of sidewalls of the floating gate 130 adjacent to the gate insulator layer 120. The intended use limitation ("where etching processes used to

fashion the sidewall insulator spacers from a spacer insulator layer, etch the spacer insulator layer faster than the gate insulator layer and the floating gate insulator layer") does not structurally distinguish the claimed invention over Hsieh's reference; an intergate insulator layer 199 disposed over exposed portions of the gate insulator layer 120, the floating gate 130, the floating gate insulator layer 135 and the sidewall insulator spacers 195; a conductive control gate 200 disposed over the intergate insulator layer 199 and covering about half of the floating gate (col. 4, lines 17-67, col. 5, col. 6, lines 1-10, and fig. 2j).

Regarding to claim 2, the structure wherein the semiconductor region is a silicon region (col. 4, lines 17-18).

Regarding to claim 3, the structure wherein the substrate is a silicon containing substrate (col. 4, lines 17-18).

Regarding to claim 4, the structure wherein the gate insulator layer is a thermally grown oxide layer grown to a thickness of about 50 to 200 angstroms (col. 4, lines 23-24).

Regarding to claim 5, the structure wherein the conductive floating gate is composed of polysilicon (col. 4, line 25).

Regarding to claim 6, the structure wherein the floating gate insulator layer is a grown polysilicon oxide layer (col. 4, line 46).

Regarding to claim 7, the structure wherein the spacer insulator layer is an oxide layer (col. 5, lines 29-45).

Regarding to claim 9, the structure wherein the spacer insulator layer is a deposited oxide layer (col. 5, lines 16-17), the gate insulator layer is a thermal oxide layer (col. 4, lines 17-21), and the floating gate insulator layer is a polysilicon oxide layer (col. 4, line 46).

Regarding to claim 11, the structure wherein the intergate insulator layer is an oxide layer (col. 6, line 1).

Regarding to claim 12, the structure wherein the conductive control gate is composed of polysilicon (col. 6, lines 5-6).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,465,841 to Hsieh et al. in view of the remark.

Regarding to claim 8, Hsieh discloses the claimed invention except for the spacer insulator layer is a PECVD oxide layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the spacer insulator layer is a PECVD oxide layer since it was known in the art that the spacer insulator layer is a PECVD oxide layer.

Regarding to claim 10, Hsieh discloses the claimed invention except for the structure wherein the etching processes used to fashion the sidewall insulator spacers from the spacer insulator layer are an anisotropic dry etch leaving some of the spacer insulator layer everywhere followed by a wet etch leaving only the sidewall insulator

spacers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the etching processes used to fashion the sidewall insulator spacers from the spacer insulator layer are an anisotropic dry etch leaving some of the spacer insulator layer everywhere followed by a wet etch leaving only the sidewall insulator spacers.

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran